

REMARKS

In the outstanding Official Action, claims 1-14 were rejected under 35 USC 102(b) as being anticipated by Westergren et al, for the reasons of record. In this regard, it is noted that the patent number cited against the claims, namely U.S. Patent No. 6,115,409, is not Westergren, but rather Upadhyay et al. However, since a different patent number, corresponding to Westergren, is provided in the Notice of References Cited, in the interest of advancing prosecution it is assumed that U.S. Patent No. 5,423,076 is intended.

In response to the rejection, all of the independent claims have been amended in order to more clearly and precisely distinguish the novel features of the instant invention, and it is respectfully submitted that the currently-pending claims, as herein amended, are clearly patentably distinguishable over the cited and applied reference for the reasons detailed below.

More particularly, as described in the instant specification, the invention is based upon the idea of using a common main component, namely a digital synthesizer driven phase locked loop, in both the transmitting mode and the receiving mode, with this single component being in a modulating state in the transmitting mode and being in a oscillating state in the receiving mode.

It is recognized that the independent claims, as previously


presented, did not recite the important limitation of a single digital synthesizer driven phase locked loop, an important feature of the instant invention which provides low cost, simple construction and good performance, as detailed on page 2 of the instant specification. Accordingly, the Westergren reference, which clearly contains two different phase locked loop elements, was cited as an anticipatory reference. As clearly noted in the Action, Westergren, in Fig. 1, shows two different phase locked loop components, namely items 38 and 57 as identified in the Action.

In order to overcome the anticipation reference based upon the two phase locked loop circuit of Westergren, all of the independent claims have been amended to more clearly and precisely recite a single digital synthesizer driven phase locked loop. This limitation is clearly supported by the instant specification and is shown in the drawing, and is clearly described as an important feature of the invention which provides a low cost transceiver which is simple in construction but nevertheless offers good performance.

In view of the foregoing, it is respectfully submitted that the currently-pending claims, as herein amended, are clearly patentably distinguishable over the cited and applied reference for the reasons detailed above. Accordingly, allowance of the

currently-pending claims is respectfully submitted to be justified at the present time, and favorable consideration is earnestly solicited.

Respectfully submitted,

By   
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